Karlsruhe Institute of Technology

Institut fuer Technik der Informationsverarbeitung

Dr.-Ing. Jens Becker *(jens.becker@kit.edu)* **M. Sc. Matthias Stammler** *(stammler@kit.edu)*

Communication Systems and Protocols

Exercise 1

General Information
Communication Systems and Protocols (Exercises)

Matthias Stammler, M. Sc.
Institut fuer Technik der Informationsverarbeitung (ITIV)
Building 30.10, Room 218
Email: stammler@kit.edu, csp@itiv.kit.edu
Website: https://www.itiv.kit.edu/21_7686.php

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Jakob Matthias Stammler, M. Sc.

Wissenschaftlicher Mitarbeiter

Group: Prof. Becker

Room: R2.18
CS 30.10

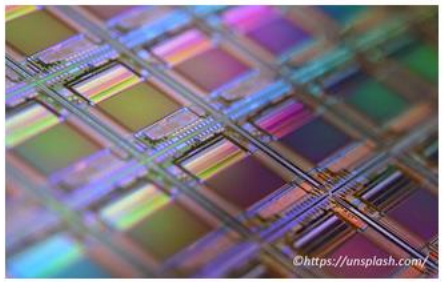
Phone: +49 721 608-41322

stammler∂kit edu

Engesserstr. 5
76131 Karlsruhe

Research interests

Monitoring of safety security-relevant incidents



Making stochastic components certifiable

Graceful Degradation strategies

Open Master Thesis Topics

Reconfigurable Monitoring of AXI messages

MA

Masterarbeit

BA

Bachelorarbeit

Eingebettete Elektronische Systeme

Umfeld:

Most newly engineered cars these days contain a large number of different ECUs and bus systems to communicate between them. The development effort to make these communication systems safe and secure is steadily increasing. When applied safety and security mechanisms fail, the result could be catastrophic, as demonstrated in 2015, when a Jeep Cherokee was remotely accessed without the need for physical contact with the vehicle or any user input. Monitoring the car's communication and these attacks is important to mitigate the errors made in future projects.

Aufgabe:

The task of this master thesis is to design, implement and test a reconfigurable monitoring module and strategy for Xilinx FPGAs, that can collect all messages on the AXI bus and save them. The module should be able to ignore specified messages and only save messages that don't adhere to the given rules. The rules should be able to change during operation. The presence of the monitoring platform should not be noticeable by other components inside the FPGA.

Voraussetzungen:

- Very good knowledge of VHDL, Verilog (through HSC, DHL, or similar lectures) or alternatively in HLS languages such as SystemC, SystemVerilog or Chisel
- Knowledge of object-oriented languages, such as Java, C++
- Knowledge of communication systems (through CSP or similar lectures)
- Before the start of the concrete work, an exposé has to be written and approved by the supervisor.

Bei Interesse bitte melden bei: Matthias Stammler, R218 / stammler@kit.edu

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Schedule CSP

Monday: 09:45 – 11:15 (NTI)

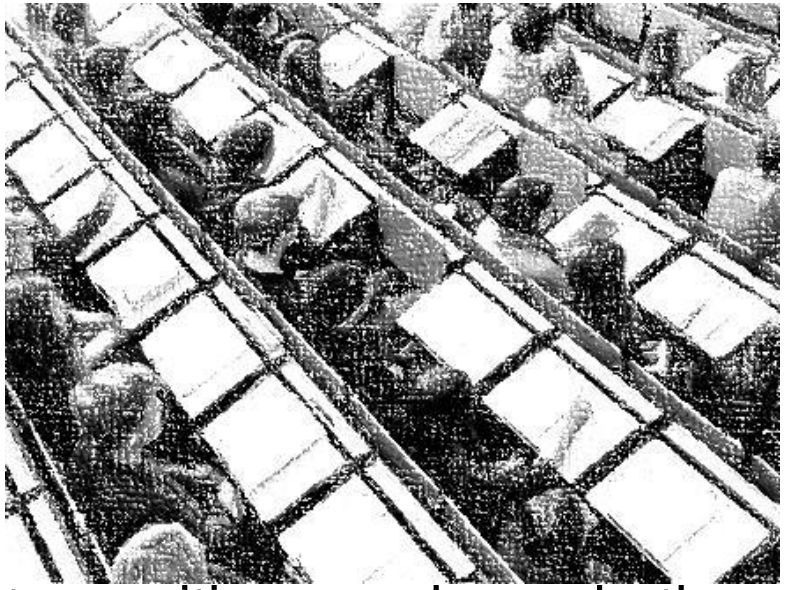
- 18.04.2022 – Easter Monday
- 25.04.2022 – Lecture 2
- 02.05.2022 – Exercise 1
- 09.05.2022 –
- 16.05.2022 – Exercise 2
- 23.05.2022 – Lecture 7
- 30.05.2022 – Exercise 3
- 06.06.2022 – Pentecost week
- 13.06.2022 – Lecture 9
- 20.06.2022 – Exercise 4
- 27.06.2022 –
- 04.07.2022 – Exercise 5
- 11.07.2022 – Exercise 6
- 18.07.2022 – Exercise 7
- 25.07.2022 –

Thursday: 09:45 – 11:15 (NTI)

- 21.04.2022 – Lecture 1
- 28.04.2022 – Lecture 3
- 05.05.2022 – Lecture 4
- 12.05.2022 – Lecture 5
- 19.05.2022 – Lecture 6
- 26.05.2022 – Ascension Day
- 02.06.2022 – Lecture 8
- 09.06.2022 – Pentecost week
- 16.06.2022 – Corpus Christi
- 23.06.2022 – Lecture 10
- 30.06.2022 – Lecture 11
- 07.07.2022 – Lecture 12
- 14.07.2022 – Lecture 13
- 21.07.2022 – Question time
- 28.07.2022 –

Written Examination

- Date: Monday, 01.08.2022
- Time: 11:00 – 13:00
- Place: Audimax, Fasanengarten (preliminary)



- No examination aids are permitted, except for:
  - A ruler
  - A non-programmable calculator
  - a single sheet of A4 paper with self- and hand-written notes, writing may be on both sides OR two sheets of A4 paper with writing on one side each.
  - A dictionary
- The language of the examination is English

Ilias Learning platform

- Contents:
  - Lecture and Exercise slides
  - Forum
  - Student surveys
  - Taskbook
  - Old examinations
  - Calendar
  - General announcements
  - Link to the live stream

- Please visit regularly

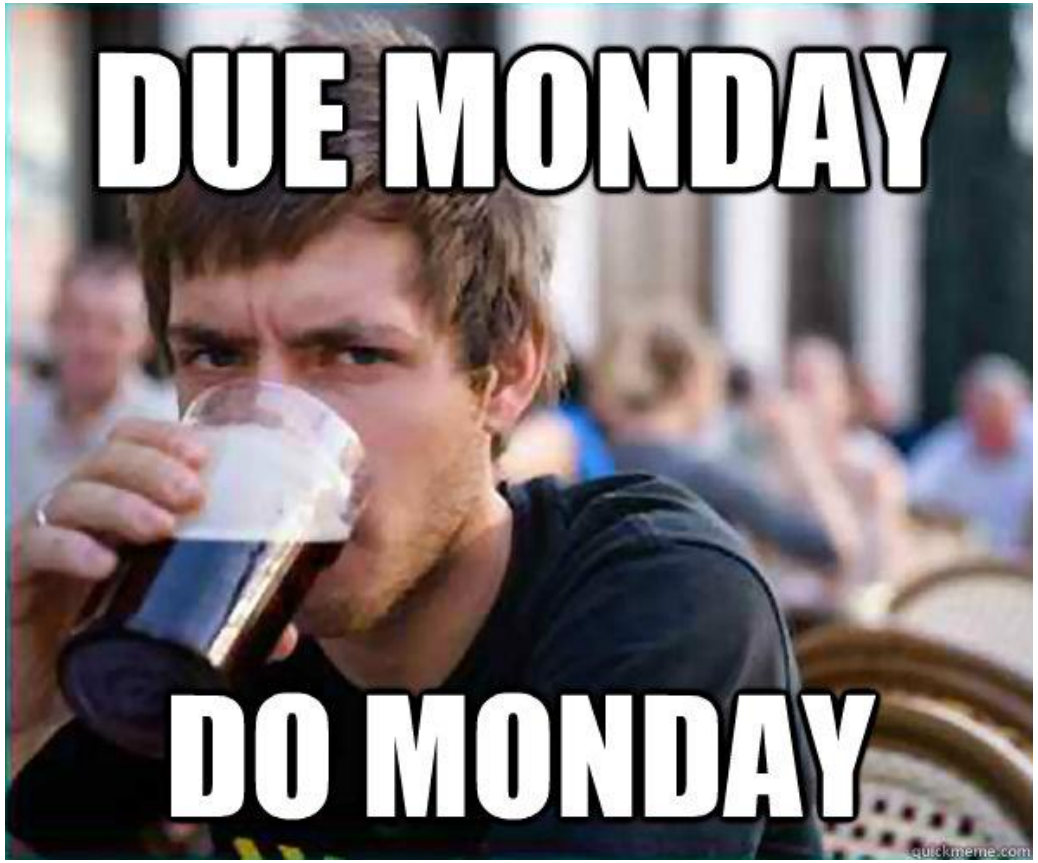
Format of Exercises

- Each exercise date contains tasks and includes
  - Overview of topic relevant to the task
  - Description of task
  - Time to solve the task
  - Discussion of possible solutions

- Questions are welcome at any time
- Please speak English, so that everyone understands the question
- After each exercise, the notes will be uploaded to ILIAS

Format of Exercises

- The tasks are provided roughly one week prior to the exercise
- It is recommended to work on them before and keep the tasks ready
- There will be time in the exercise itself to work on the tasks
- Some tasks are printed before

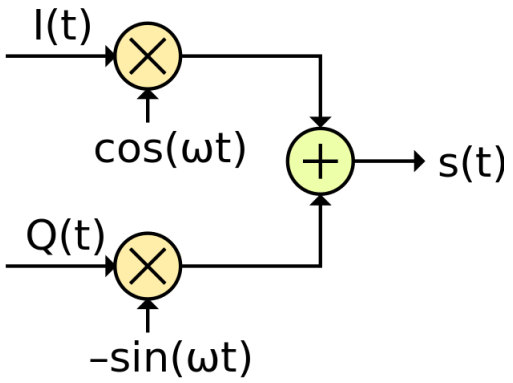


Task 1: Quadrature Amplitude Modulation

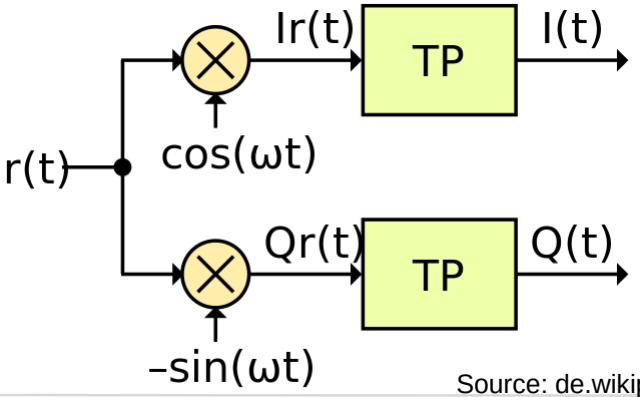
Quadrature Amplitude Modulation (QAM)

- Usage of two sine carrier signals that are shifted 90° to each other → Signals do not interfere with each other
  - One signal is called In-phase component (I)
  - Other signal is called Quadrature Component (Q)
- These two signals are added up to form the sender signal (IQ-Modulation)
- Demodulation requires same phase in sender and receiver → additional measures required

QAM-Modulation



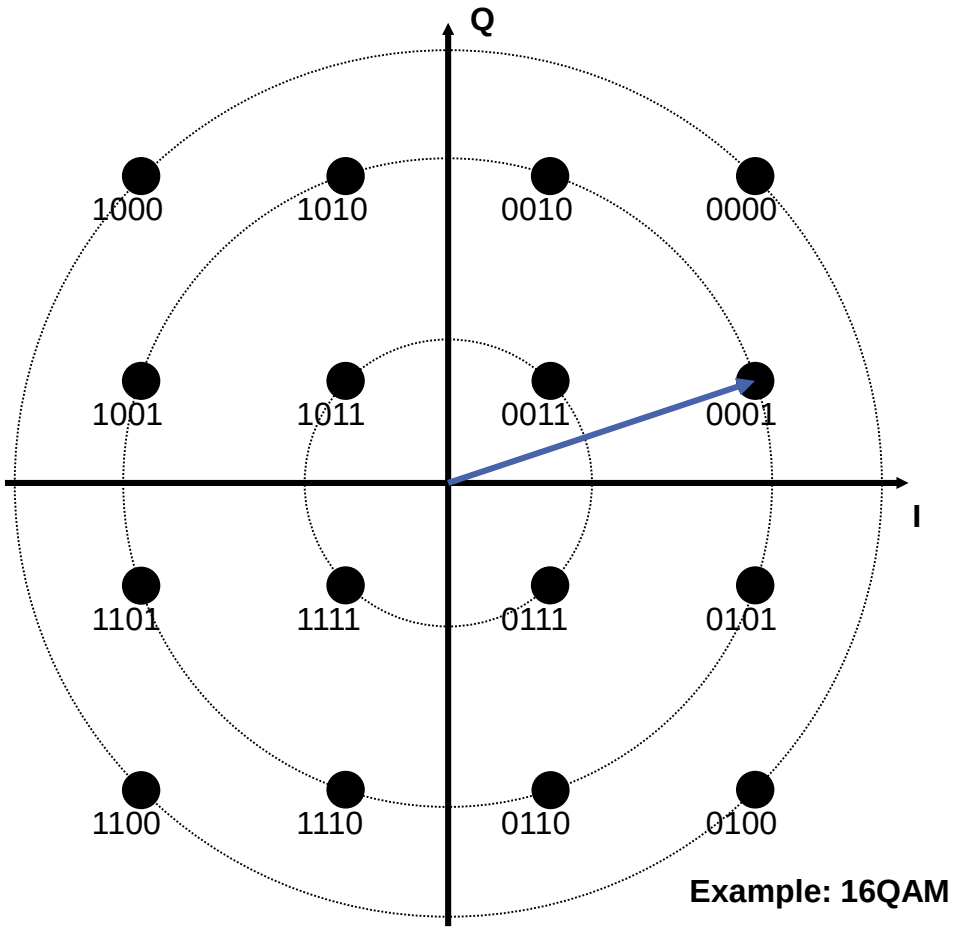
QAM-Demodulation



Source: de.wikipedia.org

Quantizied QAM: Constellation diagram

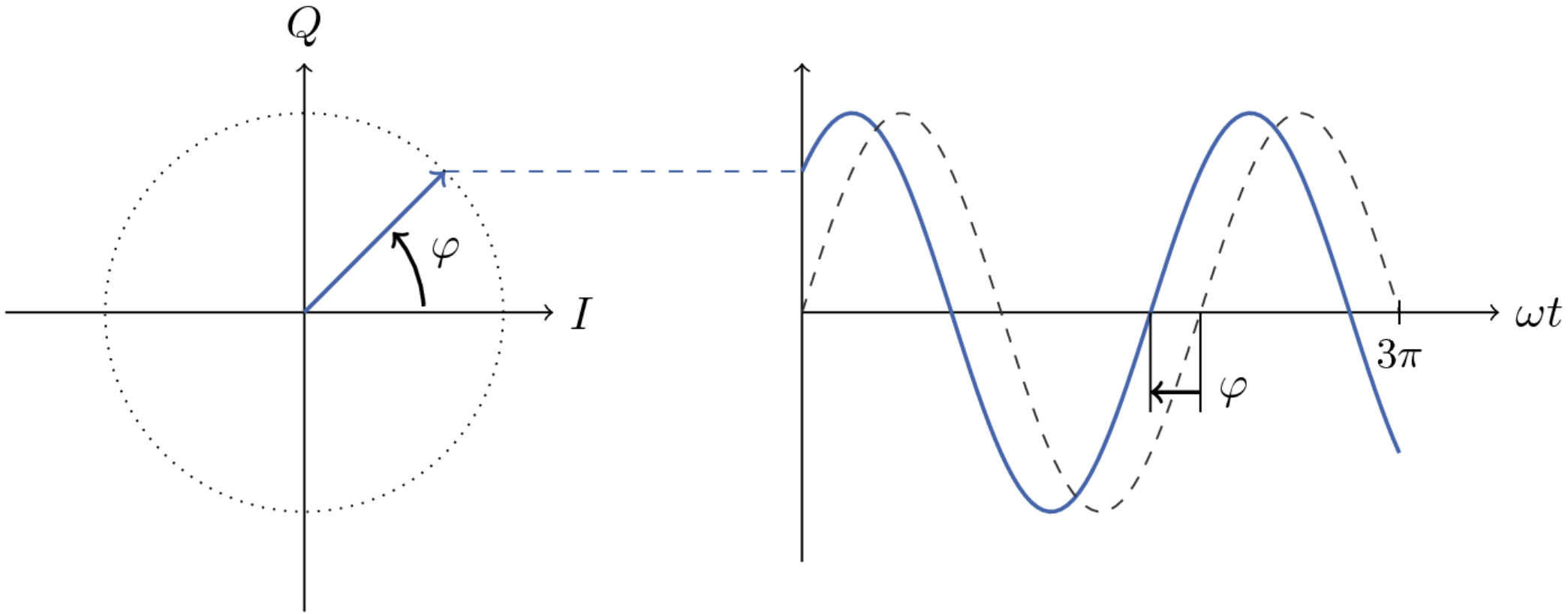
- The two QAM carriers can be represented in a two-dimensional diagram → **constellation diagram**
- When using discrete and independent signals, each point in the constellation diagram can represent more then one bit



Example: 16QAM

Constellation diagram

- Angle corresponds shift



QAM: placement of constellation points

- Signal is influenced by noise during transmission
  - Received signals are not at the ideal positions
  - Acceptance radius is required to define valid ranges for each point

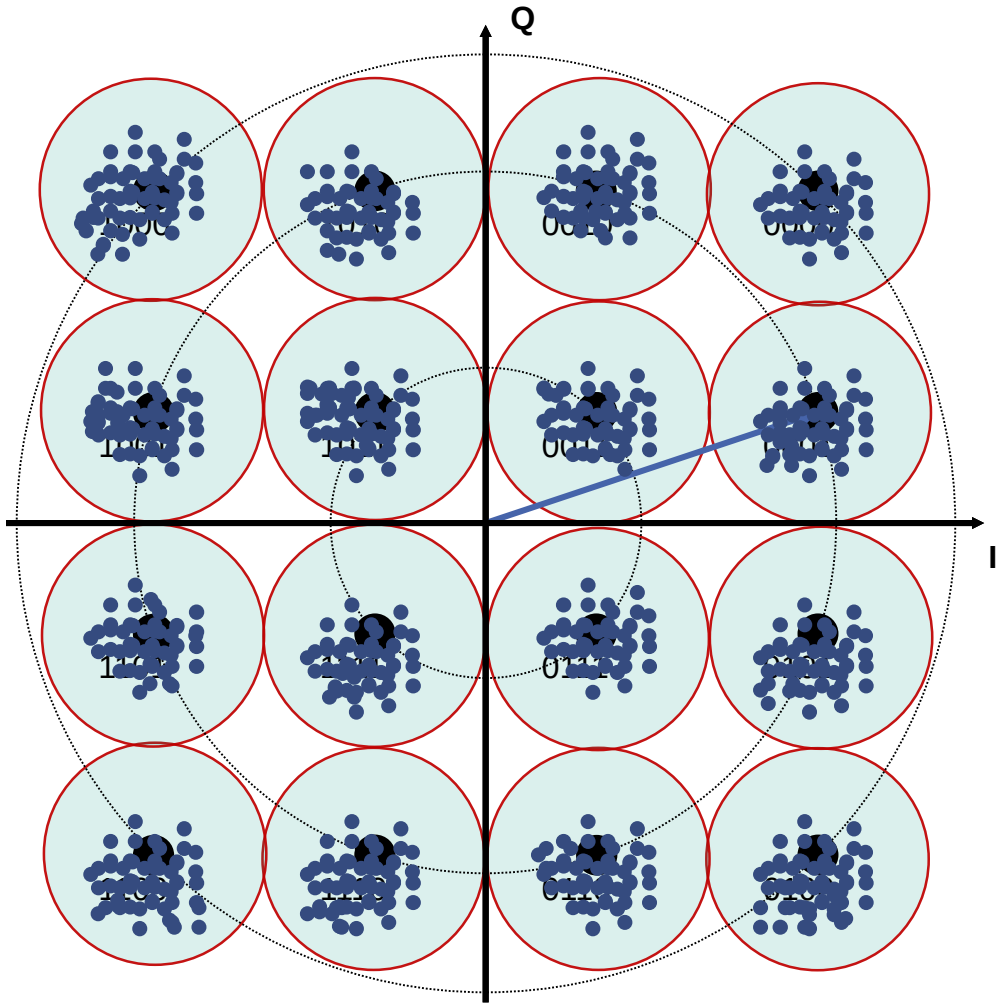
Positioning of signal points:

- Maximize distance of points to avoid misinterpretation of a signal

In General:

- More points allow more bits per signal (higher data rates) but require better signal-to-noise ratios

→ Trade-off required



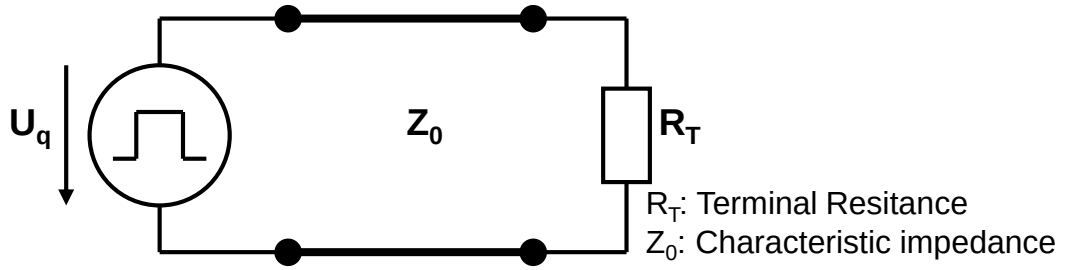
Task 1: Quadrature Amplitude Modulation

Time allocated 10 min

Task 2: Reflections on Wires

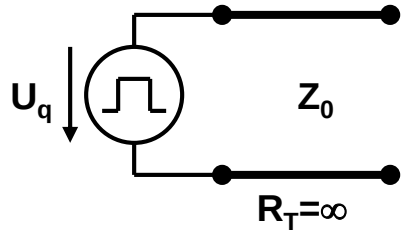
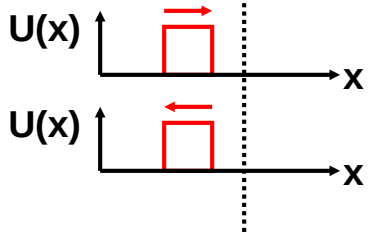
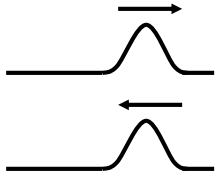
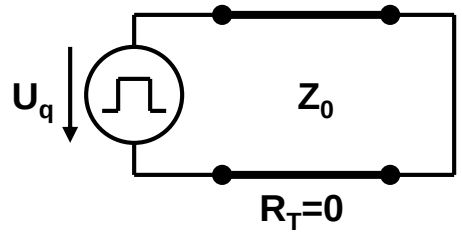
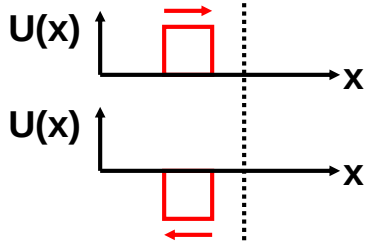
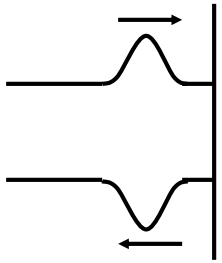
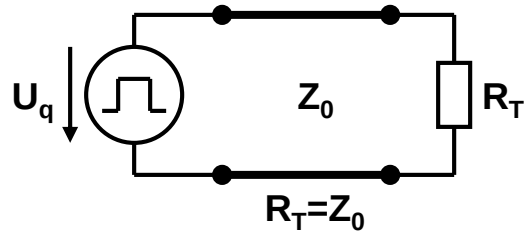
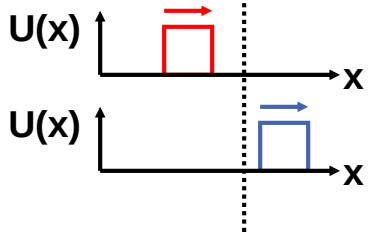
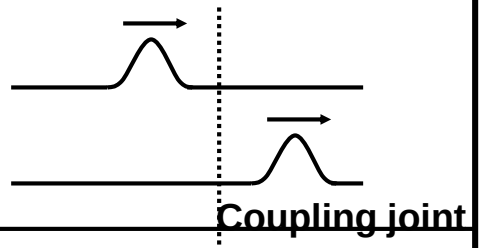
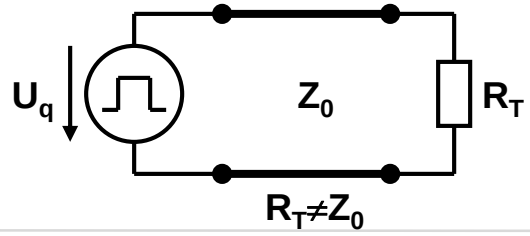
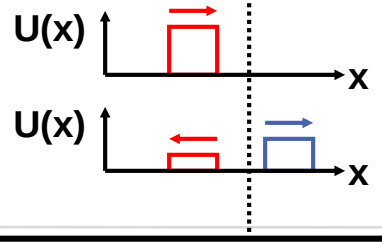
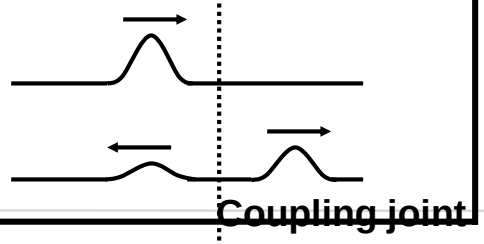
Reflection at the wire end

- Signals spread wavelike within long lines/wires
- There exists a forward and eventually a backward running wave that interfere on the wire
- The amplitude of the backward running wave depends on
  - The impedance of the line
  - The terminating impedance at the end of the line

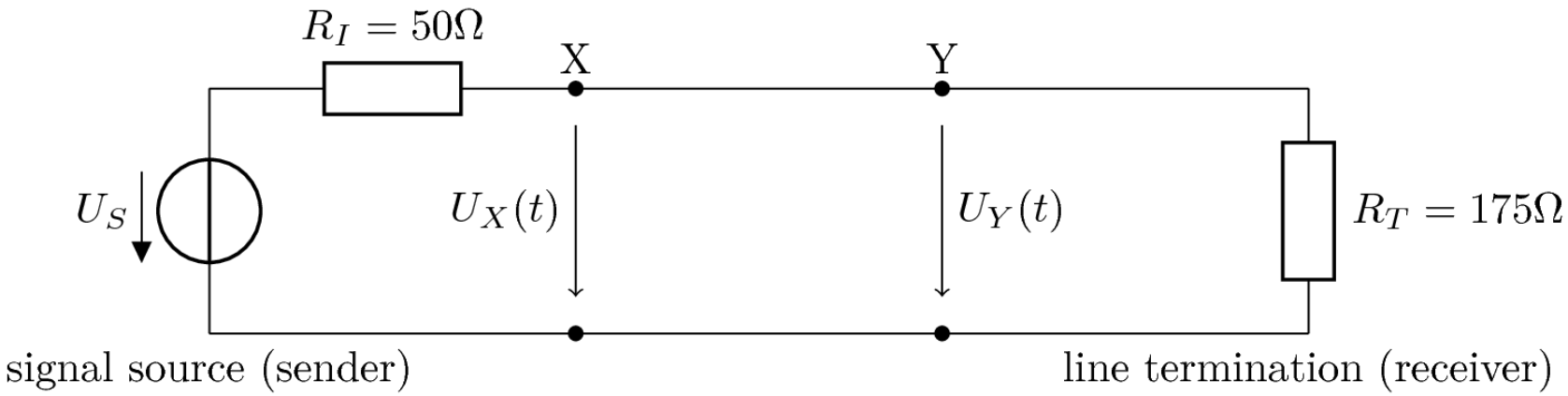


- Definition of the reflection factor: $r = \frac{R_T - Z_0}{R_T + Z_0}$

Reflection on wires

Line	Reflection factor r	Voltage curve	mechanical analogue
	r=1		 loose end
	r=-1		 solid end
	r=0		 Coupling joint
	-1<r<1		 Coupling joint

Task 2: Reflection on Wires

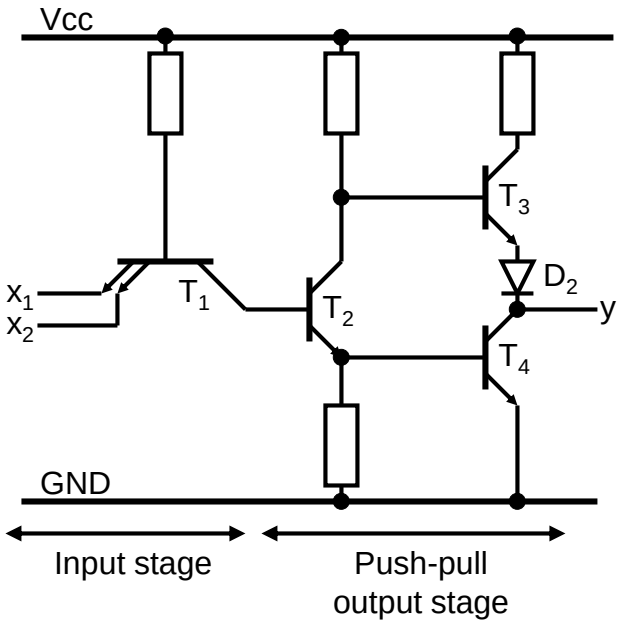


Time allocated 15 min

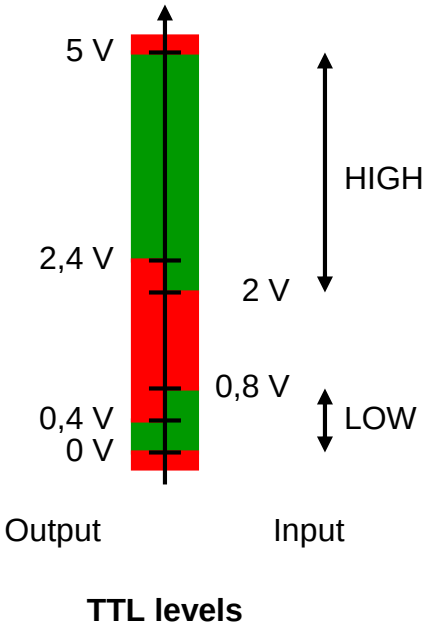
Task 3: TTL Technology

Electrical Output Driver

- Transistor-Transistor-Logic (TTL)
  - In earlier times the most common used technology
  - Inverted Transistor 1 at input provides high input resistance
    → low load for previous circuit
  - Output transistors T3 and T4 are only conducting one at a time



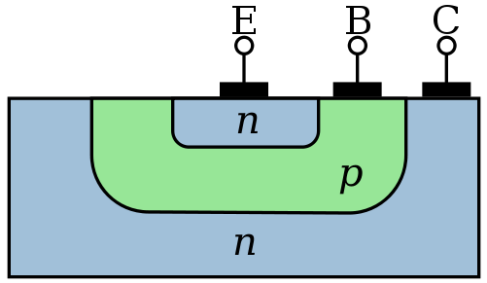
TTL basic gate (i.e. SN 7400)

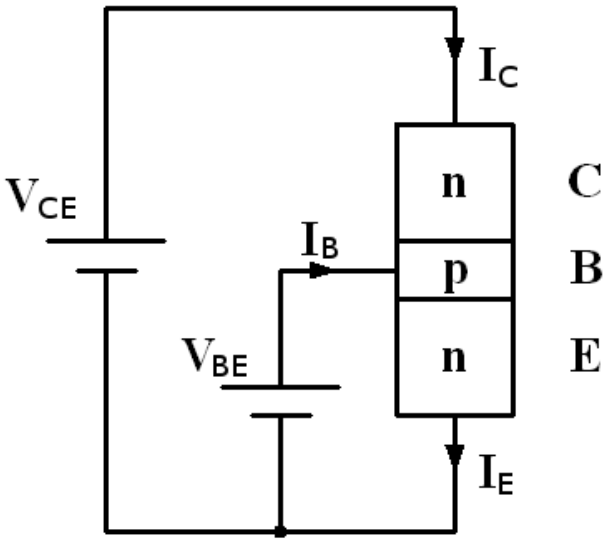


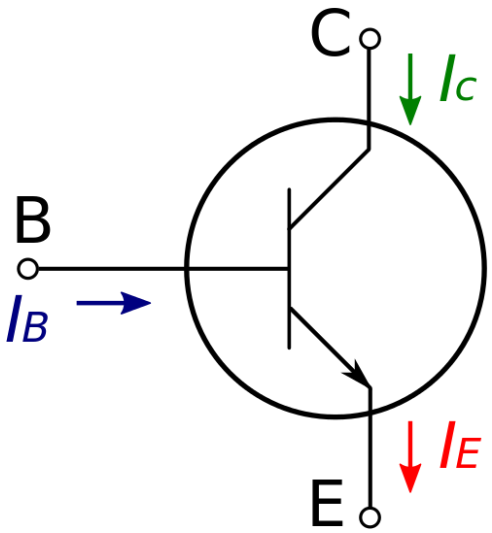
TTL levels

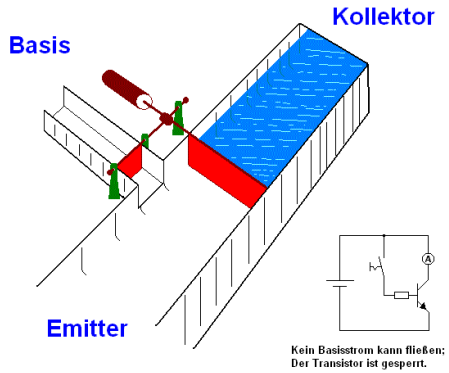
Bipolar junction transistor

- NPN
  - layer of P-doped semiconductor (the "base") between two N-doped layers
  - when there is a positive potential difference measured from the base of an NPN transistor to its emitter, the transistor becomes active

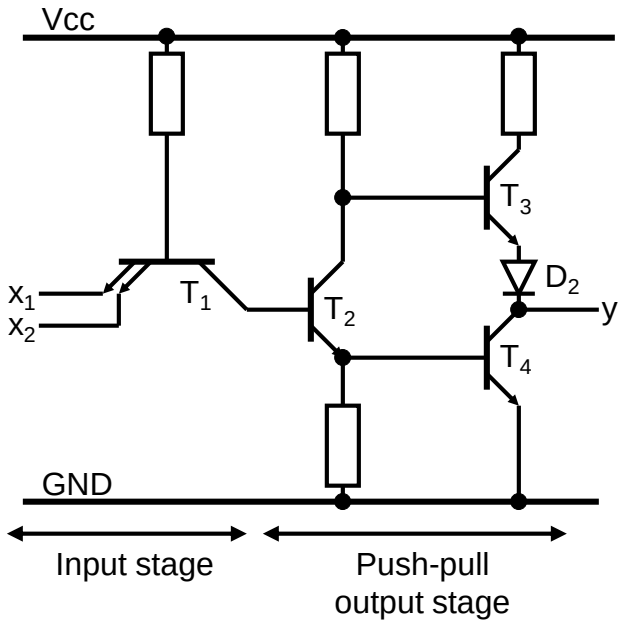








Task 3: TTL Technology



Time allocated 5 min